#### **REMARKS/ARGUMENTS**

This Amendment is responsive to the Office action dated February 23, 2005, setting forth a shortened three month statutory period for reply expiring on May 23, 2005. A petition for a three month extension of time and associated fee are filed herewith, extending the period for response up to and including August 23, 2005.

Claims 1-19 are pending in the application, with claims 1, 6 and 10 being independent claims. In brief review, the Examiner objected to Fig. 1, objected to the specification at page 10, rejected claims 10-19 as not enabled, and rejected claims 6-9 as indefinite. The Examiner also rejected claims 1-4, 6, and 10-19 as anticipated, and rejected claims 5, 7-9 as obvious.

By this Amendment, claims 1-3, 5-6, 8-11 and 17 have been amended and claim 4 has been cancelled. Reconsideration of the application and claims is respectfully requested.

#### RESPONSE TO OBJECTION TO FIG. 1

The Examiner required that Fig. 1 be designated with a legend "prior art." Fig. 1 has been labeled "PRIOR ART" on a replacement sheet that is attached hereto. Accordingly, this objection to the drawing should be withdrawn.

## **OBJECTION TO THE SPECIFICATION**

The Examiner objected to the specification at page 10, as "inconsistent in discussing which elements comprise the positive feedback loop." The specification has been amended at page, 10, lines 3-4, to be consistent with page 10, line 21 in order to address this objection and consistently list the elements that may be included in one example of a positive feedback loop. Accordingly, it is respectfully requested that this objection to the specification be withdrawn.

# RESPONSE TO NON-ENABLEMENT REJECTION

The Examiner rejected claims 10-19 under 35 U.S.C. Section 112, first paragraph, as based on a disclosure which is not enabling. The Examiner states, "transistors M3, M6 and M8-M10 are deemed critical or essential to the practice of the invention but are not included in the claims." (Office Action, p. 2). This rejection is respectfully traversed.

First, it is respectfully requested that the Examiner provide a basis for his assertion that transistors M3, M6 and M8-M10 are deemed "critical or essential" to the practice of the

invention. For instance, Fig. 3 implements an embodiment of the invention without the use of transistor M10 shown in Fig. 2. In light of this, it is unclear why the Examiner believes transistor M10 is "critical or essential."

Second, the specification expressly describes the embodiment recited in claims 10-19, so the specification does provide an enabling disclosure of this embodiment. See the specification at p. 5, lines 11-25, which states:

According to another embodiment of the present invention, disclosed herein is a circuit providing a current reference. In one example, the circuit includes a current mirror including a first transistor (e.g., M5) and a second transistor (e.g., M4); at least one resistor (e.g., R1+R2) defining a voltage node (e.g., Vtn); a pull-down transistor (e.g., M3); and an output transistor (e.g., M7); wherein the first transistor (e.g., M5) is coupled with the at least one resistor (e.g., R1+R2) and provides an amount of current thereto; wherein the second transistor (e.g., M4) is coupled with the output transistor (e.g., M7) for providing a bias signal to the output transistor (e.g., M7); and wherein the amount of current provided by the first transistor (e.g., M5) into the at least one resistor is mirrored to the second transistor (e.g., M4). The load may be coupled to the output transistor such that the load receiving the current reference.

Third, the specification is not understood to state that transistors M3, M6, and M8-M10 are critical or essential to the operation of the invention recited in claims 10-19. For instance, with regard to transistors M3 and M8, the specification states at p. 9, lines 16-19 "[i]n one example, the negative feedback portion of the circuit, which may include transistors M3, M5, M8, and R2, R1 . . ." (emphasis added). The language of the specification states that transistors M3, M5 may be part of one example of the invention. And as argued above, Fig. 3 implements an embodiment of the invention without the use of transistor M10 shown in Fig. 2.

For at least these reasons, the specification enables the embodiment of the invention recited in claims 10-19, and it is respectfully requested that the non-enablement rejection of claims 10-19 be withdrawn.

# RESPONSE TO INDEFINITENESS REJECTION

The Examiner rejected claims 6-9 as indefinite under 35 U.S.C. Section 112, second paragraph as lacking antecedent basis for the phrase "floating mirror" in claim 6. Claims 6, 8-9 have been amended to correct this minor informality, and accordingly it is respectfully requested that this rejection be withdrawn.

### RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. SECTION 102

The Examiner rejected claims 1-4 and 6 as anticipated by U.S. Patent application publication U.S. 2001/0022527 "Semi-conductor Device" in the name of Hosono, et al. (hereinafter the Hosono publication). This rejection is respectfully traversed.

#### Claims 1-4

Claim 1 as amended recites, in part, a "circuit for generating a reference current, comprising: a positive feedback loop coupled with a floating current mirror; and a negative feedback loop diverting current from the floating current mirror, wherein the circuit operates with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages." The Examiner interprets Fig. 1 of the Hosono publication as anticipating this claim, however, the Examiner does not state where in the Hosono publication is it shown that the Hosono circuit operates "with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages" as recited in claim 1. For at least this reason, claim 1 and dependant claims 2-3 are believed to be allowable over the Hosono publication.

#### Claim 6

Claim 6 as amended recites, in part, a "method for providing a current reference, comprising: providing a current mirror circuit portion; providing a positive feedback loop portion coupled with the current mirror circuit portion; providing a negative feedback loop portion diverting current from the current mirror circuit portion; and operating the current reference with a minimum supply voltage of approximately the sum of a transistor threshold voltage plus three drain saturation voltages." The Examiner interprets Fig. 1 of the Hosono publication as anticipating this claim, however, the Examiner does not state where in the Hosono publication is it shown that the Hosono current reference operates "with a minimum supply voltage of

approximately the sum of a transistor threshold voltage plus three drain saturation voltages" as recited in claim 6. For at least this reason, claim 6 and dependant claims 7-8 are believed to be allowable over the Hosono publication.

Claims 10-19

The Examiner rejects claims 10-19 as anticipated by Applicants' prior art Fig. 1. Claim 10 as amended recites, in part, a "floating current mirror including a first transistor and a second transistor." Fig. 1 of the present application discloses a current mirror having transistors M4, M5 each with their sources coupled with VPWR, which is not a floating current mirror. Because Fig. 1 does not disclose a floating current mirror, claim 10 is allowable over Fig. 1.

Because dependant claims 11-19 depend from and further limit independent claim 10, claims 11-19 are also allowable over Fig. 1.

RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. SECTION 103

The Examiner rejected claims 5 and 7-9 as obvious in view of the Hosono publication. Claim 5 is allowable because it depends from and further limits claim 1, which is believed to be allowable. Claims 7-9 are allowable because they depend from and further limit independent claim 6, which is believed to be allowable.

#### CONCLUSION

In view of the above, claims 1-5, 6-9 and 10-19 remain in the application and are believed to be allowable.

Payment for the three-month extension of time is enclosed herewith. No further fees are believed to be due with this Amendment; however, if any additional fees are required, please consider this a petition therefor and please charge such fees to Deposit Account number 04-1415.

Respectfully submitted.

**DORSEY & WHITNEY LLP** 

Date: August 23, 2005

James/A. Pinto

Attorney Reg. No. 40,774

PH: 303-629-3400 Customer No. 20686

Attachments

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# **Amendments to the Drawings:**

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes Fig. 1, replaces the original sheet including Fig. 1. In Fig. 1, the legend "PRIOR ART" has been added.

Attachments: Replacement Sheet

Annotated Sheet Showing Changes

ANNOTATED SHEET SHOWING CHANGES
CIRCUIT AND METHOD FOR IMPLEMENTING A LOW SUPPLY
VOLTAGE CURRENT REFERENCE, Atty. Dkt. No. 2059/US/2, filed
March 8, 2004, Cust. No. 20686, PH 303-629-3400



